HDD Servo Design Using the Si9990CS

Alan Grace

Introduction

Small-form factor hard disk drive (HDD) rotating memories place several difficult constraints on the designers of servo mechanisms for head positioning and spindle motor drives. The most demanding design constraint is size. There is simply not enough room in a 1.8-inch drive to include separate ICs for the head positioning and spindle servos. The Si9990CS from Siliconix addresses this space problem by combining voice coil motor (VCM) and spindle drive servos in a single 64-pin slim quad flat package (SQFP). The Si9990CS is manufactured using a BiC/DMOS process to achieve maximum integration while minimizing internal power dissipation. Bipolar transistors are used in analog circuits (such as the bandgap reference) and where the lowest operating voltage is required (such as the head retract circuit). CMOS logic allows the quiescent current to be reduced to only 1.2 mA in the sleep mode. DMOS output transistors eliminate the need for external drivers and allow rail-to-rail voltage swing.

While the size of HDDs is continually being reduced, the complexity and performance of the servos is being driven in the other direction by the need to increase areal densities. Reduced track spacing (more tracks per inch) requires greater accuracy, which translates to higher gain and dynamic range for the VCM servo. Also, minimization of the seek time and the hand-over time between seek and track following modes (which directly relate to a drive's access time specifications) requires greater bandwidth for the VCM servo. Loop compensation becomes critical as the gain bandwidth of the system is increased.

To meet the performance needs of the VCM servo, the Si9990CS incorporates a transconductance amplifier with low crossover distortion. Its output stage has four n-channel MOSFETs in an H-bridge configuration which are capable of 300 mA output current and are redesigned for class AB operation. Current feedback and loop compensation amplifiers are also included.

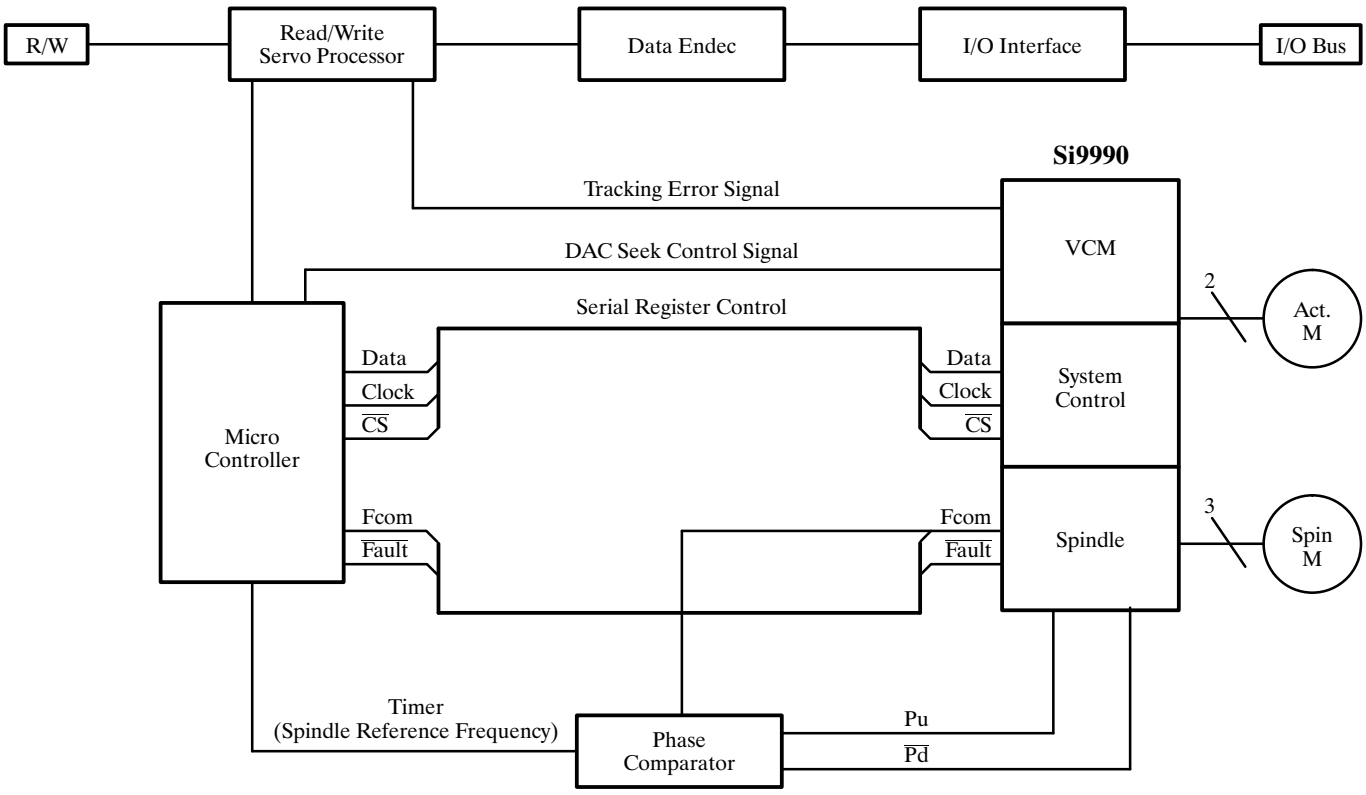


Figure 1. HDD block diagram

The push to reduce access times has also caused a trend toward higher disk rotation speeds, which places greater accuracy constraints upon the spindle servo. Although the accuracy requirements are increased, spindle position control is a repetitive task which is best accomplished by dedicated hardware. By including spindle control functions and commutation logic in the Si9990CS servo IC, the processor is freed from these tasks and can perform the system control functions for which it is uniquely suited. The Si9990CS includes three n-channel MOSFET half-bridges for driving three-phase brushless DC motors. Phase commutation is based on back-EMF sensing circuitry which eliminates hall sensors and their associated cost and assembly problems.

During normal operation there is no interaction between the spindle and VCM drive circuits: both functions are under the control of the system microcontroller. The one exception to this rule is the head retract. When power is lost, the stored kinetic energy in the spindle can be used to power the VCM and reposition the head to its landing zone. The Si9990CS incorporates an integrated disconnect switch between the upper rail voltage to the spindle and VCM drivers (V_{MOT}) and the head retract circuit's supply voltage (V_{CLAMP}). This not only eliminates an external Schottky diode, but allows both servos to operate directly from the 5-V rail. When a power failure occurs, the disconnect switch prevents the power supply from pulling down V_{CLAMP} , and integrated rectifier diodes feed the motor back-EMF energy directly to the retract circuit.

The system interfaces for the Si9990CS are relatively simple in concept (Figure 1). Microcontroller commands use a serial input bus. The VCM driver receives the tracking error signal from the read/write servo processor and the seek control signal from the microcontroller via either a DAC (digital to analog converter) or PWM (pulse width modulation) signal. H-bridge outputs, OUT+ and OUT-, drive the head actuator. The spindle driver receives two inputs from the phase comparator and feeds two output signals back to the microcontroller. The output signals are F_{COM} from the back EMF commutation circuit and a $\overline{FAULT}$ output which indicates an under voltage condition. The spindle motor is driven by outputs A, B, and C. A detailed block diagram taken from the data sheet of the Si9990CS is shown in Figure 2 for reference. Refer to the data sheet for detailed information on the device specifications.

This application note will address the operation of the Si9990CS using design examples for both the head and spindle servos. First the serial control register will be explained, along with other system control functions. Either classical or state-variable techniques can be used for the loop analysis, and the former is applied here. The track-following loop is designed first, since parameters from this loop must be accounted for in the design of the seek loop. Block diagram reduction is performed to more easily determine the transfer function of the overall loop, while maintaining correspondence to the inner control loops. Having worked out the transfer functions, parameters for a specific example are entered to complete a numerical example. Finally, the design of snubber circuits for the VCM is discussed.

A similar procedure is then followed for the spindle drive: beginning with a description of the circuit, including an explanation of back-EMF sensing. Motor startup sequence problems are covered, and then the control loop is addressed in detail. After the block diagram is reduced, a design example is worked out. Lastly, snubber design for the spindle is covered.

System Control Functions

Serial Register

Refer to tables 1 and 2 in the Si9990CS data sheet and to Figure 13 in this Application Note. The mode control input (serial register) uses three lines: DATA (six bit command word), CLK (data bit clock), and CS/ (chip select input which allows the Si9990C S to latch in the new data word). With the $\overline{CS}$ pulled low, a six-bit word is entered into the data line. Bits D0, D1, and D4 define operating states for the VCM and spindle servos. D2 and D3 program the current limit thresh old for the spindle driver, and D5 is for a factory test mode. After the data has been loaded the $\overline{CS}$ pin should be returned to a high state, at which time the Si9990CS adopts the new operating state. The recommended data loading procedure is as follows:

1. Transition $\overline{CS}$ function to low while the clock is low.
2. Start the data clock and load D5 on the clock's low to high transition.
3. Return the clock low and make the D4 bit available.
4. Load D4 when the clock transitions low to high.
5. Repeat steps 3 and 4 for bits D3 through D0.
6. Return the clock to low.
7. Return the $\overline{CS}$ pin to a high level to activate the new data.

The serial register may be reloaded at any time during normal operation. When $\overline{CS}$ is transitioned to a low state, the present data is held, and the new data (e.g., a new value for spindle current limit) is loaded when $\overline{CS}$ returns to a high level.

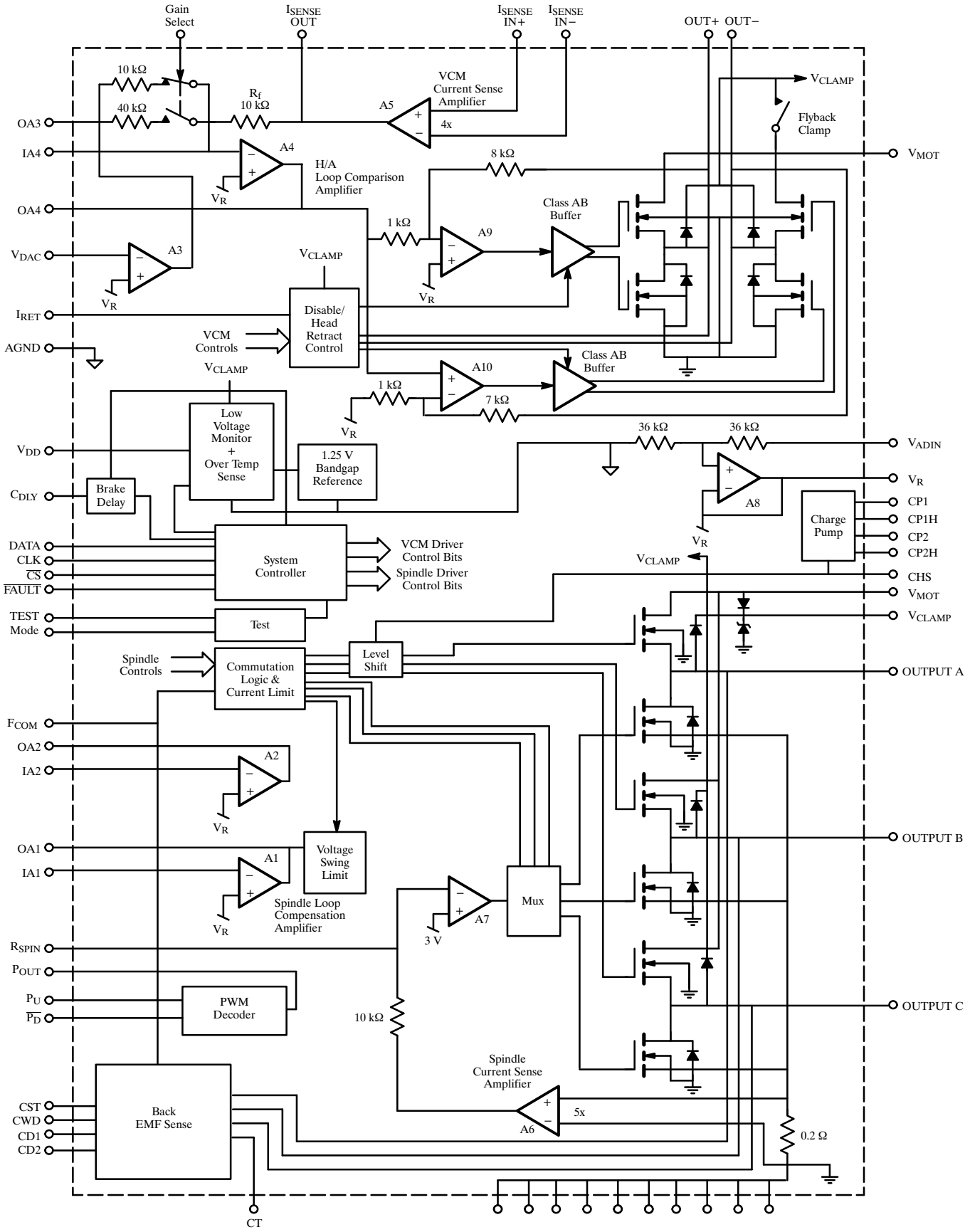


Figure 2. Si9990 Functional Block Diagram

Other Processor Control Functions

In addition to the mode control inputs from the microcontroller, $\overline{\text{FAULT}}$, F_{COM} , and I_{SENSE} OUT signals are provided for monitoring by the system microcontroller. $\overline{\text{FAULT}}$ is the under voltage flag which will be pulled low whenever the 5-V supply drops below 4.1 V typical (3.9 V minimum and 4.3 V maximum). F_{COM} pulses from the spindle drive commutation logic give position feedback to the microcontroller, which is used to determine when it is OK to read or write data. F_{COM} pulses occur N times per revolution of the spindle motor, where $N = N_{pl} \times N_{ph}$. N_{pl} is the number of motor poles and N_{ph} is the number of phases. I_{SENSE} OUT is the output from the VCM current sense amplifier, A5. It may be used for trajectory calculation in the seek mode, and it has a value of $4R_S$ volts/amp, where R_S is the actuator current sense resistor.

Voice Coil Motor

VCM Overview

The simplified schematic diagram of the VCM driver is given in Figure 3, with reference designations which are consistent with the detailed block diagram in Figure 2. The H-bridge, together with the class AB buffer drivers and amplifiers A9 and A10, comprise a transconductance amplifier with a differential gain of 16. This has been simplified to a single amplifier, A_G. The inverting input to A4 is the summing node for the track-following and seek control loop inputs, only one of which should be present at any given time. For track-following operation the parameter being controlled is the angular position, Θ (theta), and this is interchangeably referred to as the position loop. The track-following loop receives its error signal, shown as V_3, from the Read/Write Servo Processor. R_L, C_L, R_C, C_C, and R_2 form a feedback network around A4 to produce lead/lag compensation during operation in track-following mode.

A second input, V_{DAC} , to the inverting input of A3 is used for velocity control in the seek mode. The seek loop is also referred to as the velocity loop. Either a DAC or a PWM input from the microcontroller can be used for the control input during seek mode operation (Figure 4). The Si9990CS develops a reference voltage, V_R, equal to one half of the supply voltage. This buffered reference is used as the DC bias point for amplifiers A3 and A4, and is provided as an output from the Si9990CS. The DAC and tracking error signals must be referenced to this voltage. Gain switching in the transition between seek and track-following modes is accomplished using the Gain Select pin.

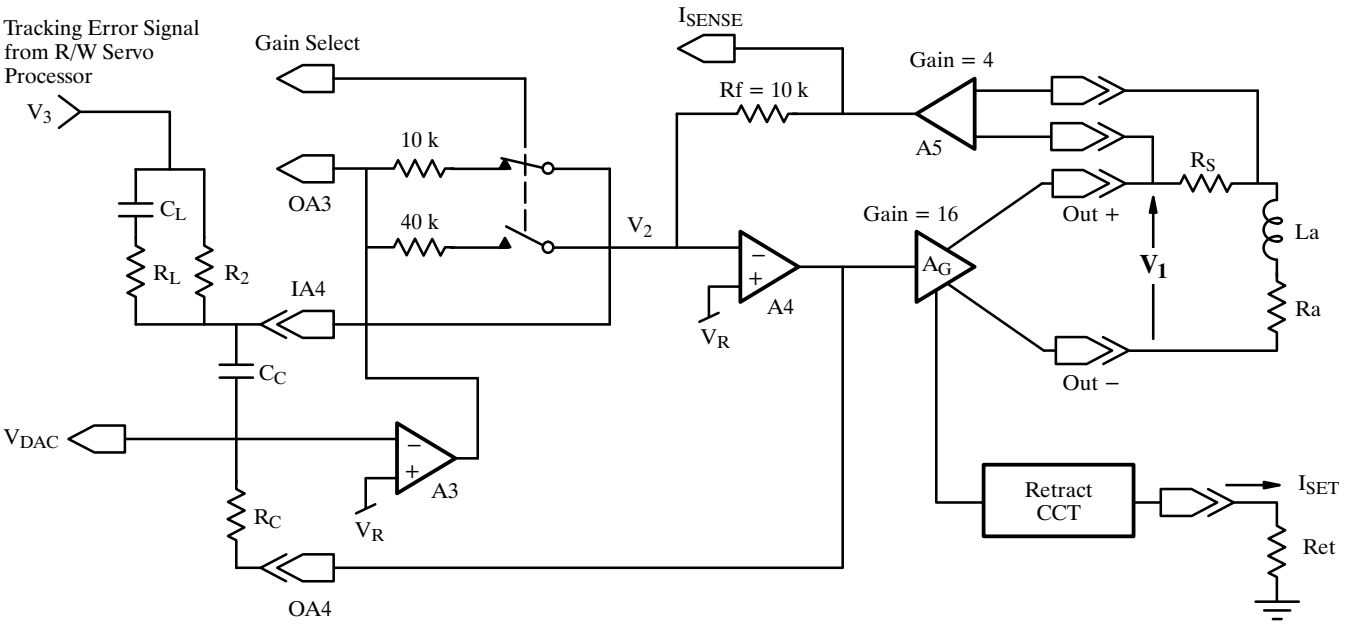


Figure 3. Simplified VCM Schematic

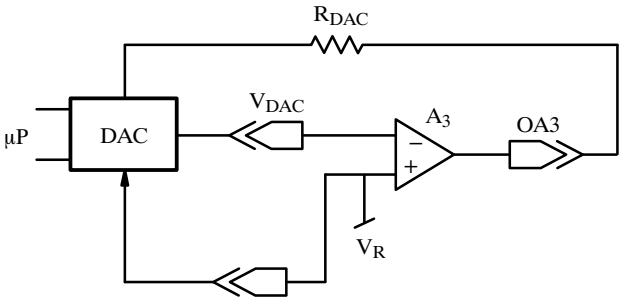


Figure 4 (a). VCM Seek Input From The Microcontroller Using DAC

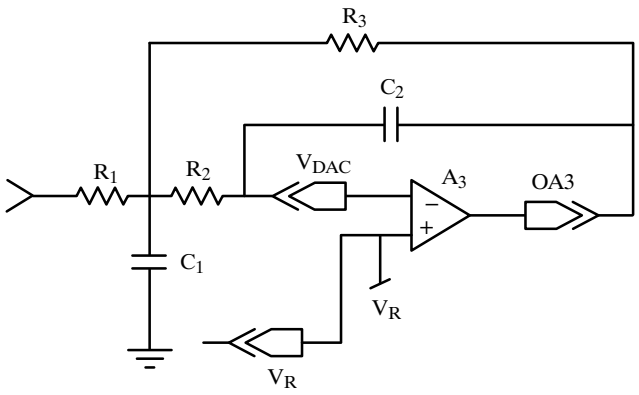


Figure 4 (b). PWM Input to Velocity Loop (Seek Mode)

The servo design approach presented here first determines the compensation for the track-following loop. This will fix the values for R_C and C_C, which place a zero in the transfer function to cancel the higher of two poles from the motor back-EMF loop. These values then remain fixed, and are entered into the minor loop compensation block (Figure 5), which is common to both loops. With two integrations plus a first order lag in the position loop, a lead/lag compensation network is required. However, the velocity loop has only one integration, and the first order pole previously chosen in the analysis of the position loop is placed more than an order of magnitude above its crossover frequency. Thus, the loop is inherently stable for all usable crossover frequencies, and a simple feedback resistor is adequate for closing the loop around A3 (Figure 4 (a)).

We have not attempted here to provide algorithms for the seek routines, although we do perform an analysis to determine the gain parameter of the velocity loop for a given bandwidth. Realization of this gain will be a combination of hardware (a resistor) and calculations implemented in firmware. Nyquist considerations are mentioned below, but system armature resonance is not. Both of these considerations, however, will limit usable system bandwidth.

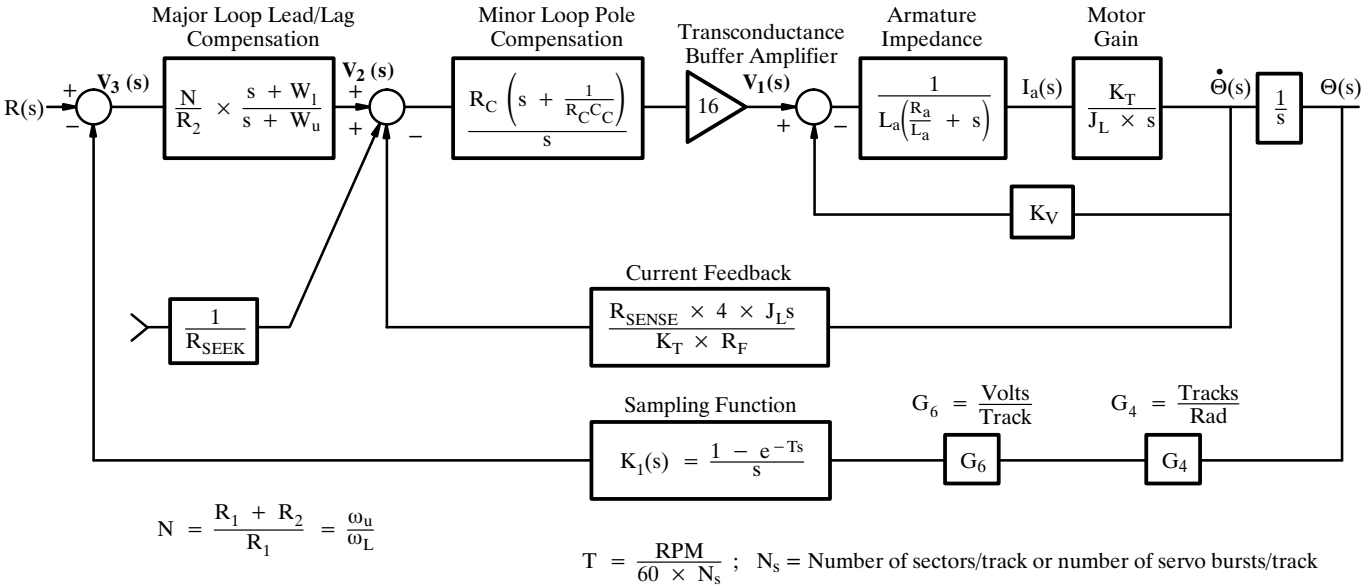


Figure 5. VCM Control Block Diagram

It does appear that sine (rather than sawtooth) profiles used in seek algorithms have a lesser tendency to excite armature resonances. The crossover performance exhibited in the Si9990CS VCM driver section addresses the often severe requirements imposed by the "flex circuit" mechanical bias, and linearity of control is maintained during transitions between velocity and position control modes.

During seek mode, the gain of the servo may be switched via the Gain Select pin. When this pin is in the high state, the gain is at its maximum value, and the voltage transference is given by

$$\frac{I_{SENSE}\ OUT}{OA3\ OUT} = 1\ \frac{A}{V}.$$

When the Gain Select pin is low, this gain is 0.25 A/V . In actuator current command terms, these gains represent $1/4R_S$ and $1/16R_s$, respectively, where R_s is the actuator current sense resistor. If needed, the I_{SENSE} OUT pin makes the actuator acceleration available for processing. The voltage out of the current amplifier is V_o , which is given as $V_o = 4 \times I_a \times R_s$ V/A, where I_a is the armature current. The acceleration, α, is given by

$$\alpha = V_o \cdot K_t/(4R_s J_L) Rad/s^2.$$

Our control loop analysis proceeds with the development of the model for the plant, after which the block diagram is reduced for the position loop. Parameters for a typical example are inserted into the resulting transfer function to further illustrate the design method.

Plant Description

The plant of the VCM system consists of the load inertia, J_L, the torque and back EMF constants, K_t and K_v, and the winding electrical parameters, L_a and $R_a \times J_L$ is a function of the geometry and mass of the actuator arm. K_t and K_v are functions of the design strategy for the armature, which must produce the required force and acceleration and yet provide counter EMF values contained within the available supply voltage. The inductance, L_a, is determined by the magnetic field distribution in the armature winding, and R_a is the electrical resistance of the armature winding. Three parameters used in the analysis are derived as follows: $G_1 = K_t/J_L$, $G_2 = 1/L_a$, $\omega_a = R_a/L_a$. The actuator arm is modeled as a two-pole system, with the terminal voltage, $V_1(s)$, as the input and the velocity, Θ (s), as the output (Figure 6(a)).The transfer function of the armature is given by Equation 1.

$$\frac{\Theta'(s)}{V_1(s)} = \frac{G_1G_2}{s^2 + s\omega_a + G_1G_2K_v} \quad (1)$$

The denominator normally represents an over-damped second-order equation with two well-separated poles, a and b. Factoring the denominator gives equation 2.

$$\frac{\Theta'(s)}{V_1(s)} = \frac{G_1G_2}{(s + a)(s + b)} \quad (2)$$

The pole at a is typically at a fraction of a Hertz, and the high-frequency pole at b occurs at a frequency on the order of 1 kHz. The phase lag of the high-frequency pole must be compensated by a zero in the forward gain block. This will be the first step in the design of the track-following loop.

Track-Following Loop

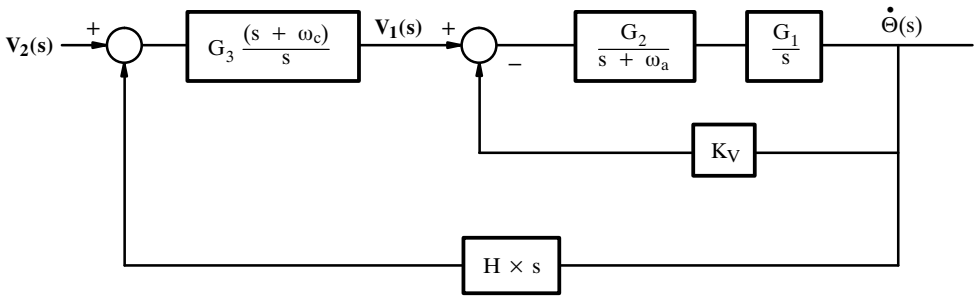
The next step is to determine the gain from $V_2(s)$ to Θ (s). A forward compensator (Minor Loop Pole Compensation Block in Figure 5) places a zero to cancel the higher frequency pole (i.e., $\omega_c = 1/(2\pi R_C C_C) = b$). This cancels the second first order lag, thus allowing a smaller compensation capacitor value to be used. Terms are defined as follows for the Current Feedback Block. R_f is the internal 10 kΩ feedback resistor through which the output from the current amplifier, A5, is summed into the control loop amplifier. R_{SENSE} is the current sense resistor. $H = R_{sense} \times G_5/(R_f \times G_1)$, G_3 is the gain to be solved for pole placement (Figure 6(a)). With cancellation of the pole at "b", the resulting forward block of the current loop then reduces to:

$$\frac{G_1G_2G_3}{s(s + a)} \quad (3)$$

Overall minor loop block then, reduces to

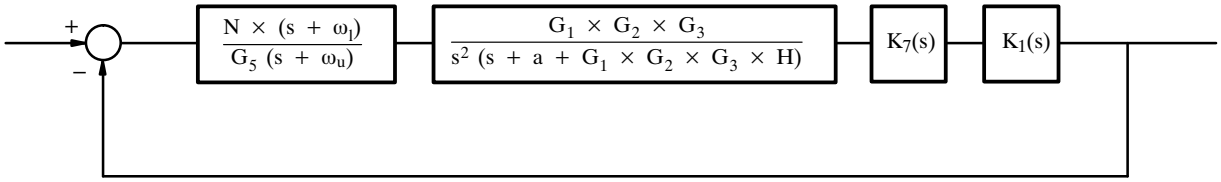
$$\frac{\Theta'(s)}{V_2(s)} = \frac{G_1G_2G_3}{s(s + a + G_1G_2G_3H)} \quad (4)$$

The position (track following) loop shown in Figure 6(b) includes the lead/lag compensation, gains, and the final integration. To complete the overall loop the following parameters are defined. ω_u is the pole and ω_l is the zero of the lead/lag compensation network. N is the gain ratio of this network. K_1 is the sample function gain, which is unity for normal choices of sampling frequency. K_7 is the conversion gain of the output function, which converts radians to number of tracks and the number of tracks to volts/track. R is the arm radius; TPI is the tracks per inch; V_{tt} is the volts/track.



$G_3 \triangleq R_c \times 16$; $G_2 \triangleq \frac{1}{L_a}$; $G_1 \triangleq \frac{K_t}{J_L}$; $H \triangleq \frac{R_{SENSE} \times G_3}{G_1 \times R_F}$ $G_5 \triangleq$ Sense Amp Gain ; $R_{SENSE} \triangleq$ Current Sense Resistor

Figure 6(a). VCM Current Control Loop Block Diagram



$\frac{\#Tracks}{Inch} \times \frac{Inches}{Radian} \times \frac{Volts}{Track} = K_7$ Volts/Radian Position – Track Following Loop

Figure 6(b). VCM Block Diagram Reduction—Unity Feedback Form

$$K_1 = \frac{(1 - e^{-sT})}{S}; \quad K_7 = R \times TPI \times V_{tt}$$

Assuming that the sampling frequency is adequate, K_1 can be neglected. The compensator gain, K_n includes K_7, G_5 and N, which is defined below. We can further simplify by including the final integration in the compensator block, and then evaluate each block separately. The transfer function for the compensator block then becomes

$$\frac{K_n(s + \omega_1)}{s(s + \omega_u)} \tag{5}$$

Define ω_x as the crossover frequency. Noting that the system has two integrations and a pole at $a + G_1G_2G_3H$, choose this pole to be at $F\omega_x$. Solving for G_3 gives

$$G_3 = \frac{F\omega_x - a}{G_1G_2H} \tag{6}$$

Substitute for G_3 in equation (4) to give

$$\frac{\Theta'(s)}{V_2(s)} = \frac{F\omega_x - a}{H \times s(s + F\omega_x)} \tag{7}$$

To guide the following parameter choice, it is necessary to evaluate the open loop transfer function at ω_x, with the condition that the gain is unity at this radian frequency. Choose N to maintain a phase margin of 45 degrees at crossover. Remember that the sampler may well introduce some phase lag, depending on the ratio of the sampling frequency to ω_x. Also, any noise filter, together with a peak detector filter, will contribute further phase lags. Thus N may need to be higher. A good minimal choice for N is 10. This will probably give the desired phase margin without sacrificing system noise performance.

With ω_x and N chosen, a solution for G_5 may be found. H could be minimally changed, as can the value of the summing resistor for the K_7 function. However, a solution for G_5 will be found with the example values given below. Set the open loop gain to unity at ω_x.

Combining (5) and (7)

$$\text{Mag.}\ \frac{K_n(s + \omega_1)(F\omega_x - a)}{H \times s^2(s + \omega_u)(s + F\omega_x)} = \text{Unity} \qquad (8)$$

Substitute for "s," and solving for K_n at ω_x:

$$K_n = \frac{H\omega_x^2(j + N^{1/2})(j + F)}{\left(j + \frac{1}{N^{1/2}}\right)\left(F - \frac{a}{\omega_x}\right)} \qquad (9)$$

VCM Design Example (cgs units)

Motor Torque Constant	K_t	=	6
Back EMF constant	K_v	=	0.024
Arm. Inertia	J_L	=	$6.3e^{-4}$
Arm. Inductance	L_a	=	$4.7e^{-3}$
Arm. Resistance	R_a	=	12
Current Sense	R_s	=	1
Sense Feedback Res.	R_f	=	$1e^4$
Sense Amp Gain	G_s	=	4
Lead Network Ratio	N	=	10
Cross-Over Freq.	ω_x	=	$400 \times 2\pi$
Actuator Arm Radius	R	=	2 ins
Tracks/Inch	TPI	=	2500
Volts/Track	V_{tt}	=	2.5

$G_1 = 9.523e^3$; $G_2 = 213$; $G_1G_2 = 2.026e^6$;
$K_7 = R^*TPI^*V_{tt} = 1.25e^4$;

$K_n = K_7^*N/G5$; $K_n = 1.25e^5/G5$; $H = 4.2e^{-8}$

The transference of the back EMF loop is:

$$\frac{2e^6}{s^2 + s \times 3.35e^3 + 4.8e^4}$$

Factoring

$$\frac{2e^6}{(s + 18.96)(s + 3.33e^3)}$$

Use $b = 2.5e^3$ (smaller C_x); a = 18.96

Next solve for the current feedback loop. Since first order pole should be absolute minimum of 10 ω_x, make F = 20.

Then $G3 = 5.98e^5$; $R_c = G_3/16 = 36.9k$;
$C_c = 1/(Rc^*b) = 0.01\ \mu F$.

From 9 Solve for K_n:

$$K_n = \frac{42e^{-8} \times 6.31e^6(j + 31.6)(j + 20)}{(j + 03.16)(20 - 7.54e^{-3})} = 0.8748$$

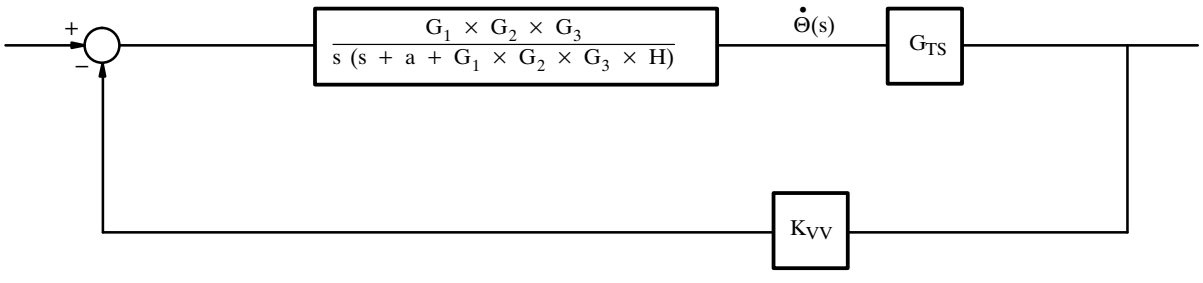
$R_2 = G_5 = 1.25e^5/0.8748 = 142k$, with N = 10,
$R_1 = 142k/9 = 15.6k$

Then lead/lag capacitor is
$C_l = 1/(3.16 \times 400 \times 2 \times \pi \times 15.6e^3) = 8.2\ nF$

VCM Seek Loop

Figure 7 shows VCM velocity loop block diagram .

The lead/lag network is not needed for loop compensation. The input from either a DAC or a PWM signal, is via A3 at Vdac input (Figure 3) . Two methods shown in figures 4 (a) and (b) indicate the needed circuitry



$G_{TS} \triangleq$ Track/Sec ; $K_{VV} \triangleq$ Volts/Track/Sec

Figure 7. Velocity Control Loop Block Diagram (VCM Seek Mode)

to accommodate the two methods. The transference of the network in Figure 4(b) is:

$$\frac{\Theta o(s)}{\Theta i(s)} = \frac{1}{\frac{s^2}{\omega n^2} + ((s \times 2\xi)/\omega n) + 1}$$

$\omega_n = [1/(R_2 \times R_3 \times C_1 \times C_2)]$;
$\xi = \omega_n \times C_2 \times [R_2 \times (1 + R_3/R_1) + R_3]/2$

A good choice for this network is to set ξ to 0.707 and ωn to a minimum of 10 times the position loop cross-over frequency.

Seek Mode/Actuator Gain

Gain: Command gain ≡ Iactuator/V(OA3) = 0.25/Rs Amps/Volt.

V(OA3) is either the PWM filter or the DAC output and Rs is the Current sense resistor.

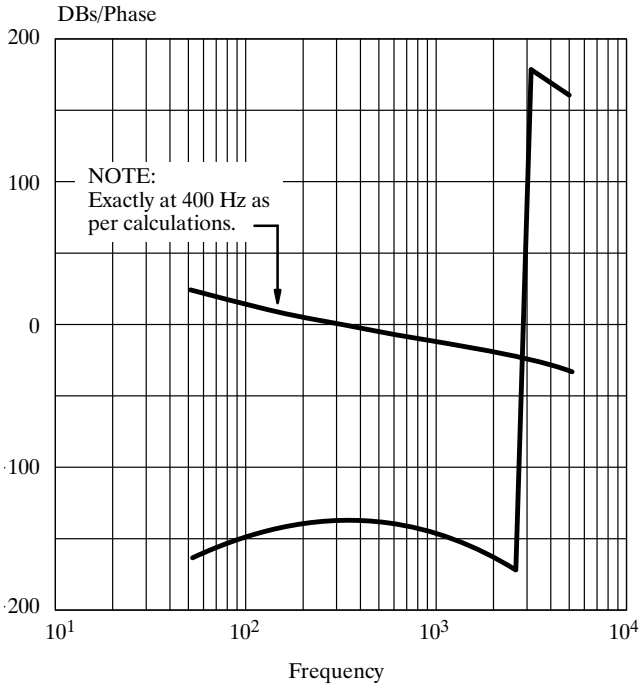


Chart 1. VCM Open Loop Plot.

Snubber Design

Actuator inductive load compensation.

Refer to data sheet for the Si9990CS Page 10.

Four components (C_{14}, C_{15}, R_{14}, and R_{15}) are shown connected from outputs OUT+ (pins 5 and 6) and OUT- (pins 9 and 10). An alternate configuration may be used. For example, a series combination of a resistor and capacitor can be connected between the out put terminals (in parallel with the actuator load).

These components compensate for the inductive behavior of the actuator load with increasing frequency. These components are important in that they suppress any tendency of the output driver to oscillate.

To choose the components, the suggested rules are as follows:

1. Choose compensating capacitor C_{14}, to resonate with the actuator inductance La at a minimum of 20 times servo cross-over frequency.
2. Choose compensating resistor $R_{14} = (4 \times La/Cc)$. This choice ensures that damping will be critical.

Example: La = 4 mH and servo cross-over is 450 Hz.

Then:

$$C_{14} = \frac{1}{(2 \text{ x } \pi \text{ x } 20 \text{ x } 450)^2 \text{ x } 4e^{-3}} = 068 \ \mu f$$

$R_{14} = (4 \times 4e^{-3}/0.068e^{-6}) = 240\ \Omega$

Note: If four components are used, two from each output to ground Cc' value must be doubled and each Rc halved.

Spindle Motor Drive

The commutation function in the Si9990CS uses an integrated solution requiring no intervention on the part of the processor to maintain spindle function. By using a combination of digital and analog techniques, the level of noise masking performance is excellent.

Status signals, Fcom and $\overline{\text{FAULT}}$, are output to the controller. Fcom indicates spindle condition in either acquisition or phase locked modes, and $\overline{\text{FAULT}}$ indicates a low-voltage condition.

Finally, the Spindle phase locked loop is controlled by an external phase comparator whose outputs (Pu and $\overline{\text{Pd}}$) control an internal charge pump, and inputs comprise a reference frequency from the processor and Fcom (motor feedback position signal).

Spindle velocity mode operation can be implemented by the processor without using the phase comparator, if the control signal is applied to IA2 via a resistor.

Commutation and Back-EMF Sensing

The method of commutation is referred to as “Back EMF Commutation.” A clocked state machine advances one “state” after each back EMF zero crossing. This clock is produced by a “Back EMF” comparator which compares the selected “off” phase induced voltage, with respect to the winding center tap.

The state machine’s outputs are decoded to switch the selected upper MOSFET transistor, and one end of the phase pair connected to it, and a lower, linear controlled MOSFET, connected to the other end of the phase pair (Figure 9 (f-h)). Note that switching only occurs to one end of the phase pair at any one time. Inspection of Phase A at the center of the On (High) interval corresponds with Phase B going off.

Figures 9 (a) and 9 (c) indicate a 30-degree lag between the comparator clock pulse and the phase switching pulses initiating the next state. Align Zc, during A(off) period. (See Figure 9 (a) and the commencement of the ramp down in Figure 9 (c).)

Capacitors CD1 and CD2 are alternately charged (positive slope) and discharged (figures 9 (b) and 9 (c)). CD1 and CD2 are caused to commence their discharge, alternately, at each zero crossing. See Zc on Figure 9 (a).

The capacitors are charged with 10 μA and discharged with 20 μA. Thus, each capacitor charges from a fixed threshold for 60 electrical degrees at 10 μA. The charge is then held at the onset of the phase switching pulse until the next back EMF pulse, at which time it discharges at 20 μA and a new phase switching pulse occurs when the fixed threshold is reached. This pulse is thus delayed 30 electrical degrees after the back EMF pulse which initiated its discharge.

When this threshold is reached, the capacitor begins to repeat the previous cycle, charging at 10 μA. The other delay capacitor is in the hold mode at this time, and in turn, will commence its discharge when the next back EMF pulse arrives.

It should be noted that the state machine produces a switching pulse only when either of the delay capacitors reaches its discharge threshold.

Motor Startup Sequence

At start, clock pulses are provided by a start oscillator until back EMF pulses are available.

Starting Conditions.

Three conditions prevail during a start operation:

1. The motor does not move. Since there is an entirely arbitrary correspondence between the state of the state machine and the motor pole/winding, inadequate torque may be produced to allow the motor to start. In this case, after a given time, another oscillator pulse advances the state machine.
2. The motor reverses. The polarity of the slope of the next Back EMF is anticipated by the state machine. If it is incorrect, the state machine is advanced after a suitable delay.
3. The motor starts and the anticipated Back EMF pulse occurs. The oscillator is inhibited, and commutation proceeds normally.

Cases 1 and 3 are straightforward. In Case 1, the oscillator continues to advance the state machine until Case 3 occurs.

Case 2, however, is not so quite so straightforward. Refer to Figure 10 (c) - (f).

In normal operation (Figure 10 (a) and (b)) the fly-back pulse **crosses** and **uncrosses** the zero crossing threshold. The next zero crossing is the “wanted” pulse. The fly-back pulse, which returns the stored armature inductive energy ($1/2\ La*Ia^2$), to the power supply, must still occur, but its trailing edge merges with the “off” winding induced voltage, which, in this case, is the same potential at which the fly-back pulse was clamped (Figure 10 (c)).

The operation of capacitor CWD is shown in normal operation, ramping down after the trailing edge of the fly-back pulse (Figure 10 (e)). In reverse operation, it continues to charge to a fixed potential and then to discharge at the next zero crossing to its onset value, at which time a state clock pulse is output to continue commutation (Figures 10 (f) and (g)).

In the normal case, where the motor is running in the desired direction, the fly-back pulse is caused to return to its onset potential, i.e. the potential of the Back EMF wave form.

For each occurrence of a zero crossing, the start oscillator is inhibited from clocking the system. If the motor does not move, then the start oscillator will output a further pulse to advance the state machine and continue commutation until zero crossings are available.

Choosing the Start Oscillator Frequency

The torque on the motor is a Sine function of the angle between pole and the winding and the applied current.

Since all positions of pole to winding angle are possible, the average torque will be used, as shown below.

Torque: $Tm = Ip \times Kt/\pi$ (1)

Acceleration (include total inertia) $\alpha = Tm/Jl$ (2)

It is necessary to find the motor radian distance between states of the state machine, and to determine how long it takes the rotor to move this distance in response to applied current step.

Radian distance: $r = 2\pi/(Npl \times Nph)$ (3)

(Npl # of poles, Nph # of phases)

Time: $t1 = (r \times 2/\alpha)$ (4)

Thus, the maximum frequency of the start oscillator is given by:

$Fs = 1/t1$ (5)

In practice Fs should be a little lower than this.

Using the motor torque constant Kv find back EMF for motor speed at the end of one pulse.

Back EMF volts:

$V_b = Kv \times t1 \times \alpha$ (6)

An example. (Units in CGS).

$Kt = 1$, $Kv = 8e^{-3}$, $Npl = 12$, $Nph = 3$, $Jl = 7.5e^{-4}$, $Ip = 0.5$ A

$\alpha = 0.5/(\pi \times 7.5e^{-4}) = 212$ Rad/sec^2

$t1 = (4\pi/(36 \times 212) = 0.0405$ sec

$Fs = 1/t1 = 25$ Hz

$Vb = 8e^{-3} \times 0.0405 \times 0.212 = 0.0686$ V

Choose CD1 and CD2.

Calculate the time between states at the running speed of the motor.

Time between states:

$Ts = 60/(RPM \times Npl \times Nph)$

Do not use this time directly in subsequent calculations, because the motor will overshoot the running speed and it is necessary to maintain a linear system, even in the acquisition mode.

A suitable figure would be a 140% overshoot. Use Ts/1.4. Use a delta v (charge) of 2 V at 10 μA.

Therefore:

CD1 and CD2 = $(10e^{-6} \times Ts/(1.4 \times 2)$ Farads.

Start Capacitor CST.

Choosing Values for the start oscillator capacitor.

CST is charged and discharged at 5 μA, from 0.5 to 2.5 V. Thus the value of CST for 25 Hz (calculated earlier) is:

Start Capacitor value:

$CST = 5e^{-6}/(2 \times 25 \times 2) = 47$ nF.

Delay Capacitor CWD.

See Figures 10 (e) and 10 (g).

In normal operation CWD is charged with 5 μA until the "fly-back" switching pulse uncrosses the zero crossing, at which time discharge is initiated at 25 μA.

In a reverse rotation condition, the fly-back does not uncross the zero crossing, so CWD continues charging towards 2.5 V. A discharge at 25 μA is initiated either when the back EMF voltage crosses zero or when the charging voltage reaches 2.5 V. At the completion of discharge, a clock pulse is output to advance the state machine.

Thus, normal clock pulse generation only occurs, for a zero crossing, after CWD has completed its discharge. Otherwise a clock only occurs after CWD has discharged from a potential of 2.5 V or from a zero crossing of a reverse rotation wave form.

To take an example, let us assume that start oscillator frequency, the period to traverse the distance between states, is:

$t1 = 0.0405$ seconds.

Obviously this will also be true for reverse rotation, since CWD charges at 5 μA from 0.5 to 2.5 V. Using a delta of

2 V and Ic of 5 μA and, assuming that zero crossing will occur in one half this distance, then the time will be:

t1/(2) = 0.028 seconds.

Thus:

CWD = $5e^{-6} \times 0.028/2$ = 68 nF.

Spindle Overview

We present here a servo design procedure which uses a conditionally stable servo, i.e. an integrator with a zero.

We have included a set of considerations to aid in the choice of crossover frequency. When these guidelines are followed, the resulting servo has a bandwidth on the order of 10 Hz. For systems using a single platter with diameters of two and a half inches and below, motor gain is very high (Torque/Inertia ratio). In order to achieve cross-over frequencies in the region of 10 Hz, gain reducing techniques are needed. The simplest method is to design with a very low dc gain, although this approach poses some significant problems:

1. The reference for the transconductance amplifier is 3-V source, whereas all other op amp references are $V_{DD}/2$. The 3-V value is chosen in order facilitate control of the current limit and to provide a reasonable dynamic range of the input signal to the transconductance amplifier. This input commands armature current in only one direction, so any input more positive than the reference has no effect, and the voltage range above the reference is wasted! The approximate half-volt differential between $V_{DD}/2$ and 3 V forces significant error voltage offsets from the phase comparator. A dc gain of 0.25 would yield a 2-V offset, and the phase comparator output would be at 4.5 V.

2. The tri-state output at Pout (phase comp charge pump) has the upper switch connected to V_{DD}. Thus, modulation of the power supply impedance, significant value with battery powered laptops, is present at Pout. However, it is also present at $V_{DD}/2$; so if Pout's operating point is at $V_{DD}/2$ (high gain system), this modulation is common moded out.

For these reasons, use of an integrator is recommended. A second option is available, but cancellation of the power supply impedance effect is less complete. This alternative method is to divide the Fcom pulses by, for example, up to 36 for a three-phase twelve-pole motor. This method may require some rather large time constant. With an operation speed of 60 RPS (3600 RPM), cross-over frequencies of 5 Hz might be used.

Phase Comparators

The very well known phase comparator using dual D flip flops and a nand gate for reset, or similar versions thereof, can provide problems in acquisition. When out of the phase lock region, the average output is a function of the beat frequency between the reference and tach (Fcom) frequency. Under these conditions, a velocity mode prevails, an integration is lost, gain goes up, and the system oscillates near the frequency of the first-order filter about one order above the designed cross-over frequency.

This problem will tend to be more likely if high ratios of lead/lag break frequencies are used. Designs following suggestions outlined later in this note have not exhibited this problem thus far. If processor control of the Pu and $\overline{Pd}$ signals is available, and a window around the desired Fcom period is used to hold either of these signals appropriately, acquisition time is greatly improved and the potential for a "velocity" mode problem, as described above, no longer exists.

Advantages of the Si9990CS

1. VCM and Spindle functions are implemented in a small 64-pin SQFP, requiring minimal board space.

2. The full H-bridge function in the VCM, and the half bridge functions in the Spindle section, have drivers which fully utilize Siliconix expertise in power MOSFET technology. The resulting, fully integrated package results in shoot-through protection, together with switching regimes, ensuring safe operation with the inductive loads.

3. The Clamp in the VCM circuit eliminates the need for a diode, with its attendant voltage drop, thus providing more voltage during retract operation when using the stored energy (back EMF) from the Spindle Motor.

4. A very robust method is used for back EMF commutation. An effective masking operation renders the Spindle control circuitry immune to noise spikes.

5. Very low cross-over distortion performance is available in the VCM section. This feature is necessary for proper operation, when the transition from seek to track following mode occurs, where distortion currents must produce torques significantly lower than the "Flex circuit" bias.

6. The ability to provide internally all VCM and repetitive, commutation functions, the processor is thus freed to address more important functions, i.e. seek and read/write control. These latter needs fully exploit the processor's computational ability.

Spindle System Block Diagram

The inputs to spindle controller are via PU and $\overline{PD}$. These are outputs from a phase comparator of the edge controlled type. The output from such a comparator in the phase locked mode are short pulses alternately positive (Ground to V_{CC}) and negative (V_{CC} to Ground). They are thus low-energy pulses and easy to filter. This the case for a high gain system, typically one with an integrator.

These outputs are input to a tri-state switch via (PU and $\overline{PD}$) which provides a further reduction in noise, i.e. when the error is small the signal at the switch output (Pout) is in a tri-state condition. Further, when the system is either above or below the required velocity, the outputs are pulsed either from Vr to V_{CC} or Vr to ground. Thus there is no ambiguity in the dc level with respect to Vr. This ensures that a lock condition may only occur at the frequency of the reference and not a multiple or sub-multiple thereof.

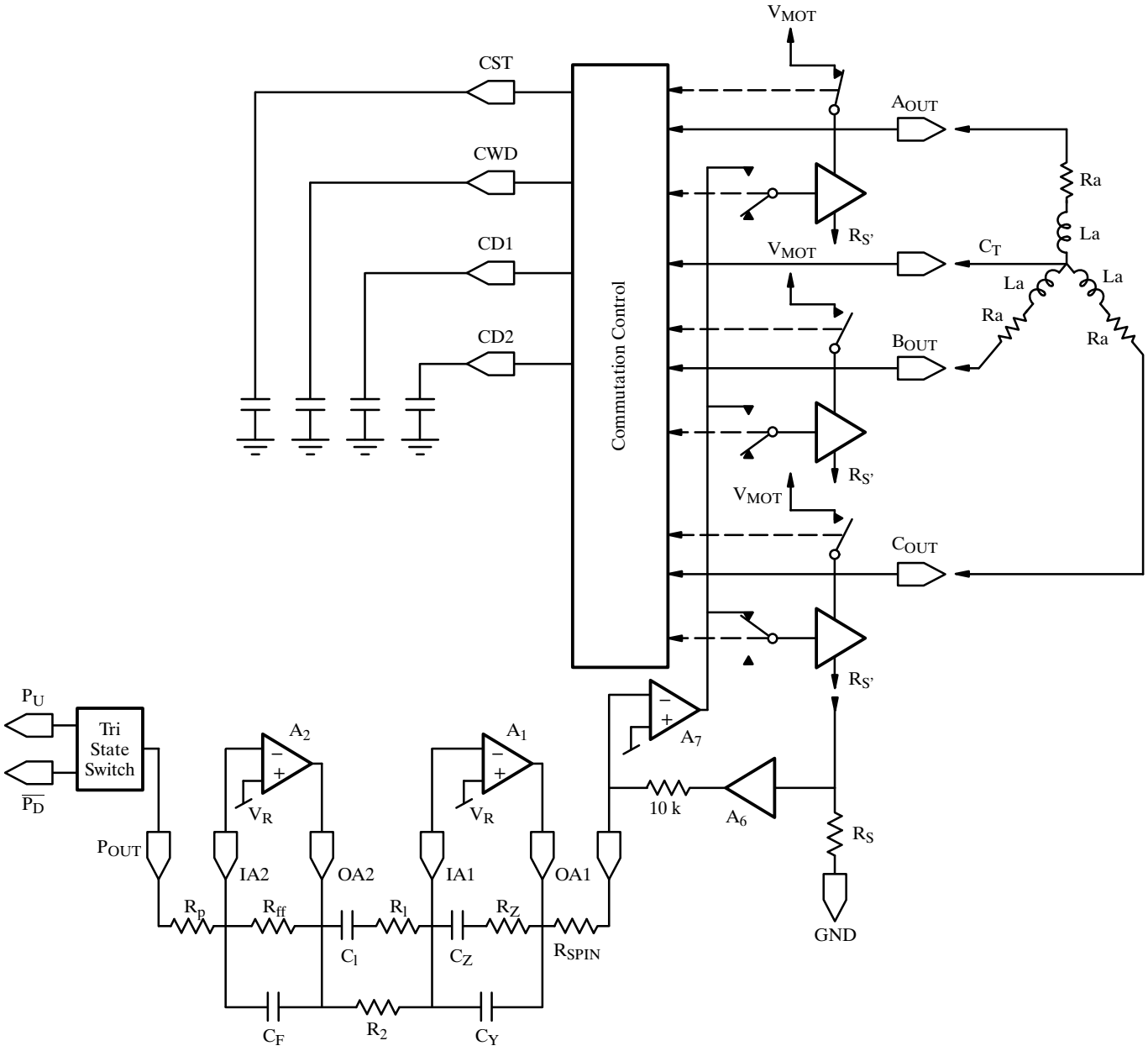


Figure 8. Spindle Driver Simplified Block Diagram

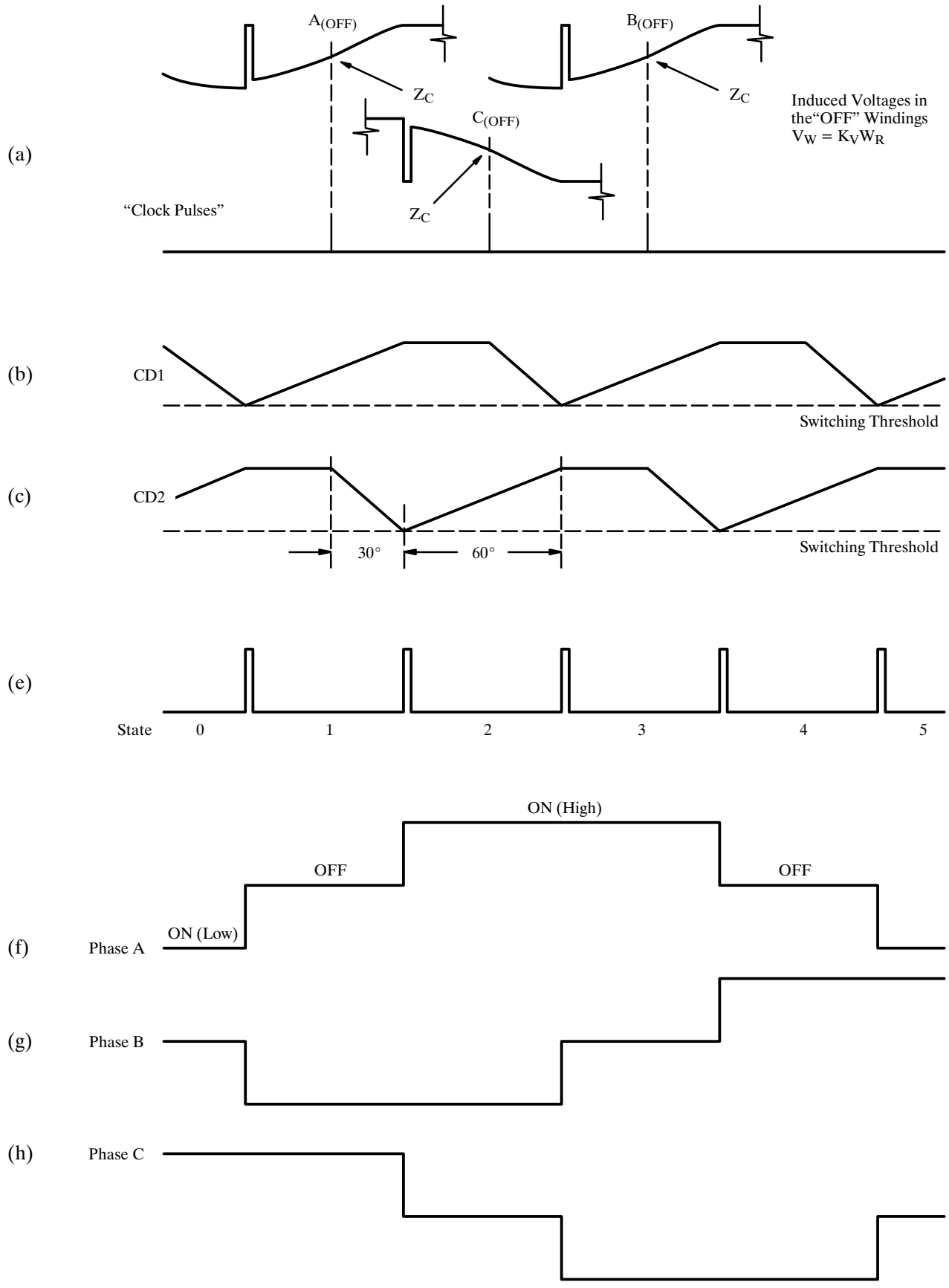


Figure 9. Spindle Driver Waveforms—Normal Operation

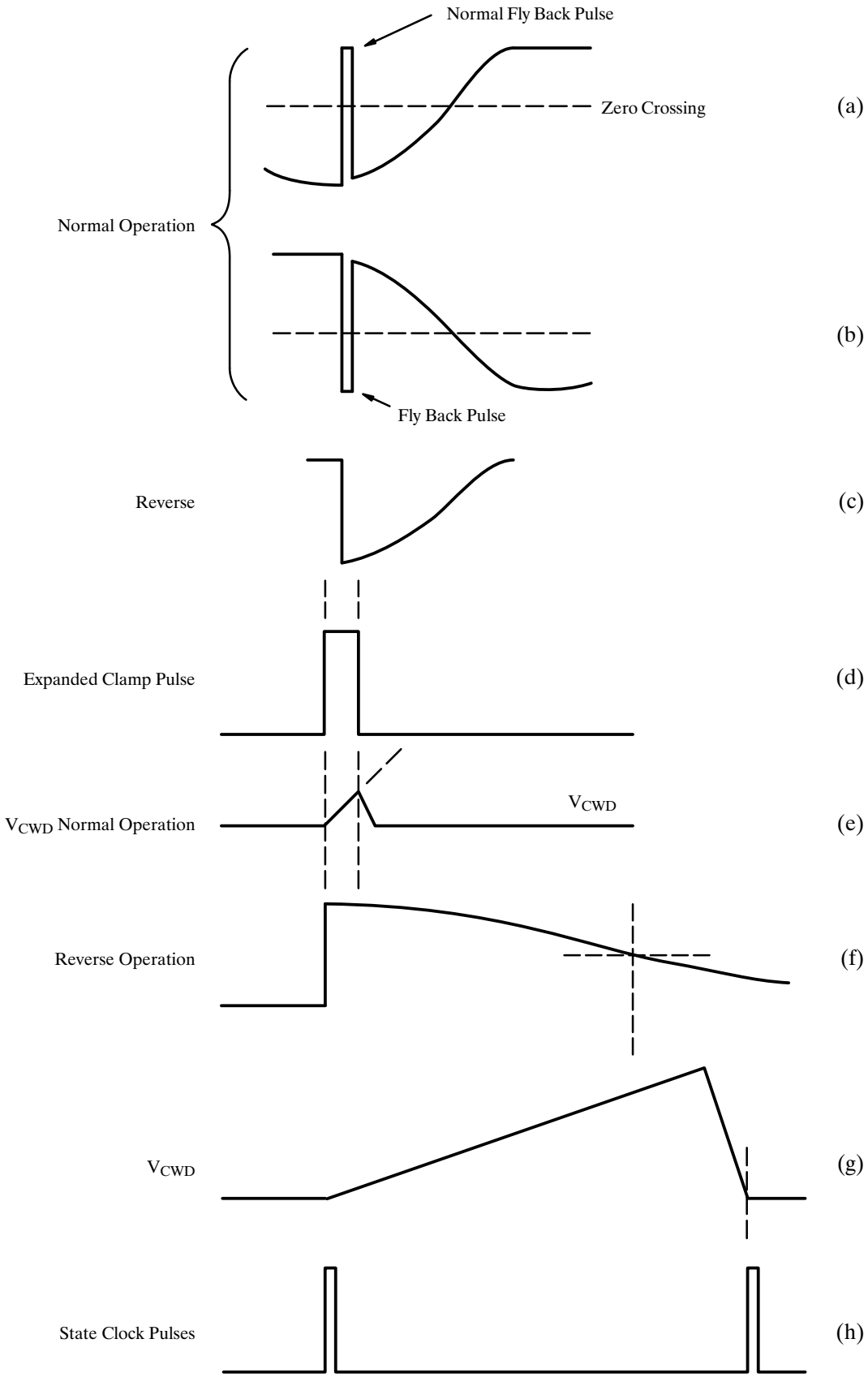


Figure 10. Spindle Driver Waveforms—Startup Operation

The output at Pout is applied via Rp and IA2 to amplifier A2. This amplifier is configured as a low pas filter. Note that there are no frequency-dependent components in the input circuit. As indicated above, when using a high gain system, the error at Pout will be essentially at V_R. Thus, voltages developed across the power supply source impedance by spindle and VCM current demands will be **common moded** out, since both the tri-state switch and V_R are supplied from VDD. Between OA2 and IA1, components R_2, Cl and Rl form the Lead/Lag network series compensator for the loop. The closure components for A1, Cz, Rz, and Cy form an integrator with zero, and a second low pass filter.

The output from A1 is fed via Rspin, to the transconductance amplifier A7. Here the output of the current sense amplifier (A6) is mixed via Rf, an internal component, with the inputs through Rspin, to set the transconductance gain . Rs (the current sense resistor) is also internal. By excellent ratiometric matching, the transconductance gain is accurately set by Rspin.

In Figure 8, the output of A7 is multiplexed to one of three output drivers. The output from the selected driver (Cout is shown in the diagram) linearly controls the "sink" current through the two series connected phases to an upper switch (Aout is shown in the diagram).

Spindle Servo Design Procedure

Design of a Conditionally Stable Servo

Suggested Rules:

(a) Cross-over Frequency = ω_x

1. Make integrator zero $\omega_z = \omega_x/10$

2. Lead n/w gain ratio $N = \omega_u/\omega_l$

3. Make lag n/w break $\omega_u = (N) \times \omega_x$

4. Make lead n/w break $\omega_l = \omega_x/(N)$

Choose N(12 - 14). Choose Noise Filter poles, ω_p and ω_q as 10 ω_x and 15 ω_x. Since ω_p and ω_q introduce additional lags at ωx, N is chosen to provide needed compensation for an overall phase margin of 45 degrees (Figure 12 (d)).

(b) Rewrite Transfer Function in terms of ω_x, i .e $(s + \omega_l)$ goes over to $(s + \omega_x/(N))$.

(c) Equate the Transference of all blocks, Fig 12 (e), evaluated at ω_x, to unity.

(d) Solve for ω_y.

(e) Evaluate component values for Fig 8.

Spindle Servo

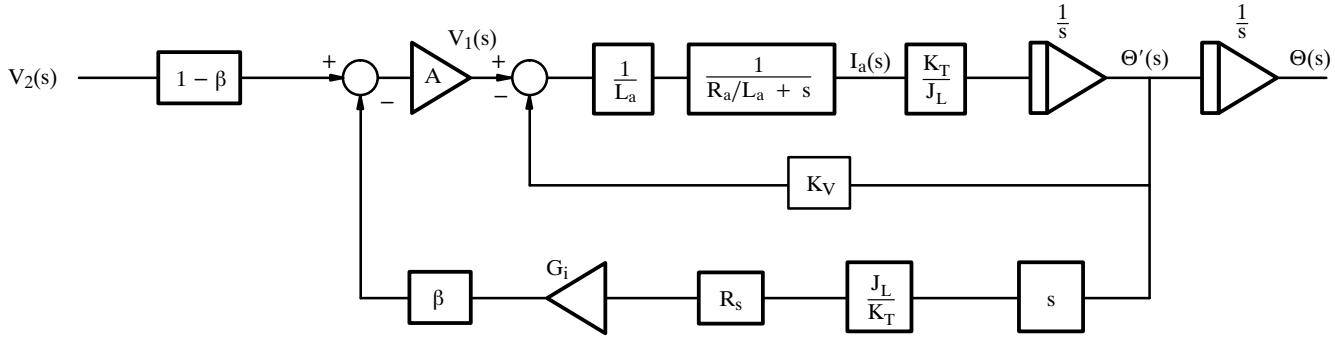
Plant

The plant for the Spindle servo comprises the motor with the following parameters:

Torque Constant Kt; Back EMF Constant Kv;
Armature Inductance La; Armature Resistance Ra;
Rotor and Load Inertia J_l

Define: $G1 = K_t/J_l$; $G2 = 1/L_a$; $\omega a = R_a/L_a$

The suggested procedure is to reduce the minor loops from Figure 11 to an equivalent block (Figures 12 (a), (b) and (c)).



$$G_1 = \frac{K_T}{J_L}\ ;\quad G_2 = \frac{1}{L_a}\ ;\quad H = \frac{G_i \times R_s \times \beta}{G_1}\ ;\quad \omega_a = \frac{R_a}{L_a}$$

Figure 11. Spindle Control Loop Block Diagram

Rather than using the simplification of ignoring the back EMF and inductance parameters of the motor and simply using the transconductance gain times the error volts and the motor torque constant, the entire loop is included in this analysis for completeness.

The reduction to block (c) in Figure 12 results in a transference which may appear to be influenced by the variability of the open loop gain of the transconductance amplifier. If, however, an evaluation of the function magnitude is made at omega (ω) = to unity, it will be evident that the magnitude function, changes imperceptibly when A, the open loop gain, varies from, say, 10 K to 50 K.

The current feedback loop uses sensed motor current with the "pick off" point moved forward to the velocity output Θ(s). The inverse of the forward functions traversed to this point are then inserted in the return loop. For example, K_t/J_l and 1/s in the forward loop go over to $s \times J_l/K_t$ in the return loop.

The reduction of the Back EMF block becomes a quadratic function yielding an over-damped solution, with a pole well above a normal spindle servo bandwidth, and a sub-radian pole, approximating a first order lag if the high-frequency pole is disregarded.

Block Diagram Reduction

Reference Figure 12 (b).

Back EMF Loop.

$$\frac{\Theta'(s)}{V1(s)} = \frac{G_1G_2}{s^2 + s\omega_a + G_1G_2Kv} \quad (1)$$

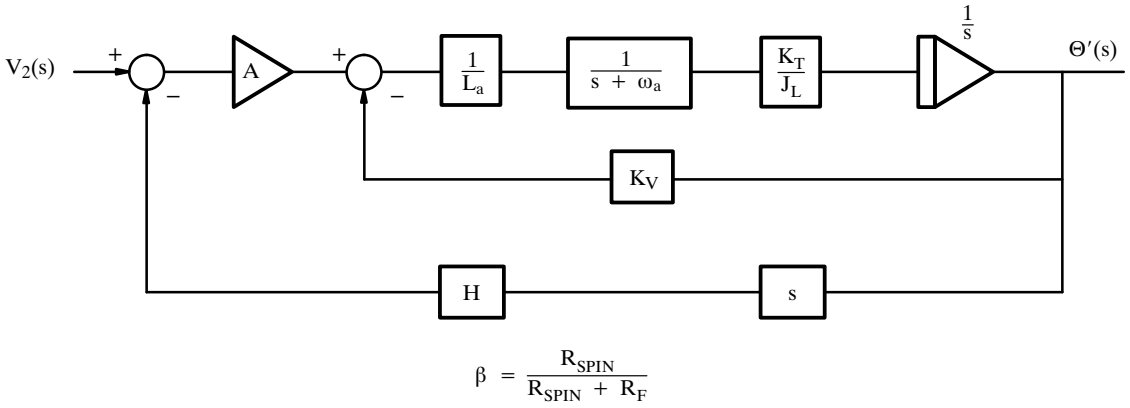


Figure 12(a). Spindle Control Loop Block Diagram Reduction – Step 1

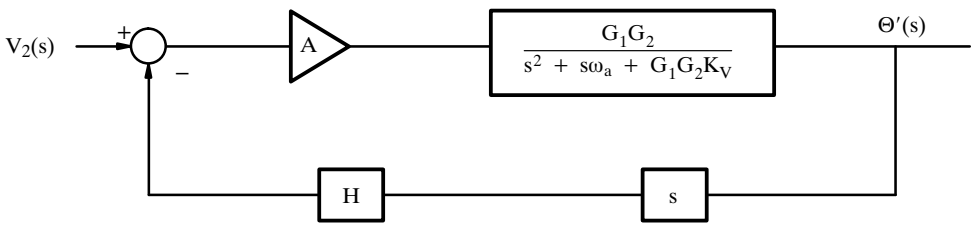


Figure 12(b). Spindle Control Loop Block Diagram Reduction – Step 2

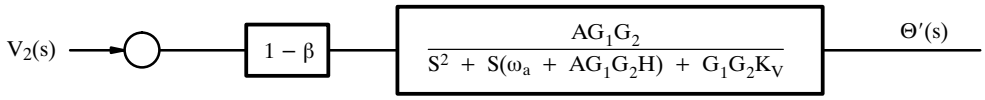


Figure 12(c). Spindle Control Loop Block Diagram Reduction − Step 3

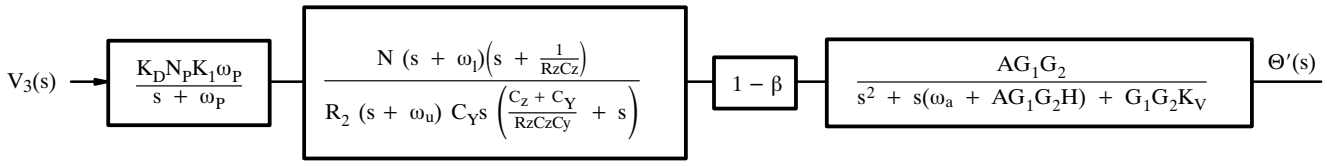


Figure 12(d). Spindle Control Loop Block Diagram Reduction − Step 4

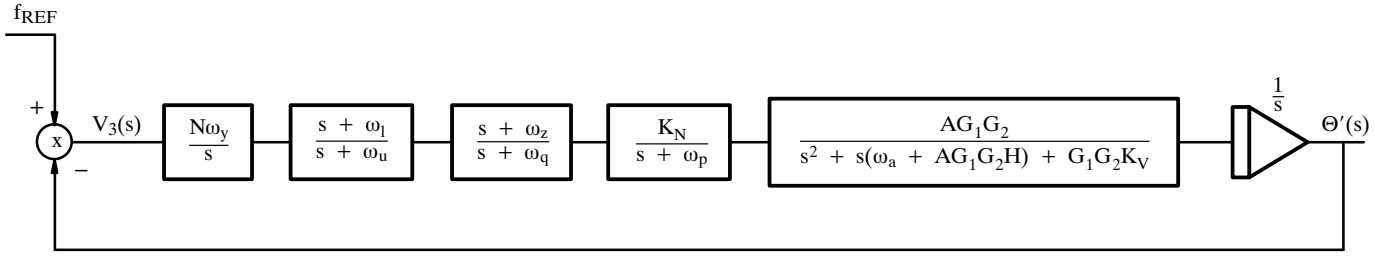


Figure 12(e). Spindle Control Loop Block Diagram Including Final Integration and Phase Comparator

Current Loop

Defining further parameters:

Current Sense resistor Rs; current sense amplifier Gi; and current loop summing ratio β; the ratio of Rspin to the internal feedback resistor Rs:

β = Rspin/(Rspin + Rf); Transconductance amplifier open loop gain = A;

H = Gi × Rs × β/Gl;

$$\frac{\Theta'(s)}{V2(s)} = \frac{AG_1G_2}{s^2 + s(\omega_a + G_1G_2AH) + G_1G_2Kv} \qquad (2)$$

Defining the remaining parameters.

Refer to Figure 12 (d).

Phase Comp Gain ≡ Kd;

First Stage Attenuation ≡ K_1;

Lead/Lag Network; Zero ≡ ω_l, Pole ≡ ω_u; N ≡ ω_u/ω_l

Compensator Gain:

$K_n = KdNpK_1(1 - B)\omega_p\omega_q N/\omega_z$;

Number Of Pulses/Rev ≡ Np;Integrator Zero ≡ ω_z;

Double Pole At Origin ≡ $1/s^2$ (Includes Output Integration); First Order Lag Filter Poles ≡ ω_p and ω_q;

Gain To Solve For ≡ ω_y; $\omega_y \equiv 1/(R_2C_y)$

Spindle System Block:

Figures 12 (d) and (e).

Transference of Compensator:

$$\frac{\omega_y \times Kn \times (s + \omega_l)(s + \omega_z)}{s^2(s + \omega_p)(s + \omega_q)(s + \omega_u)} \qquad (3)$$

Spindle Design Example

Example.:

Design a servo (conditionally stable type) to run a motor at 3600 RPM with a cross-over frequency of 10 Hz. Motor has 3 phases and 12 poles, thus there are $3 \times 12 = 36$ pulses per revolution.

The most significant perturbating sources in the motor will at the running frequency RPM/60 and, for a three phase motor, at three times the running frequency.

The upper bandwidth choices are limited by the sampling frequency and the need to attenuate the third harmonic of the running frequency. This harmonic is seen as a POSITION pulse disturbance, thus some method of averaging out this component is mandatory. Thus the bandwidth may not be chosen to be above the running frequency, in an attempt to enclose the once around disturbance because there will not be adequate attenuation of the third harmonic.

In choosing a cross-over frequency below the once-around frequency, said frequency must be low enough to attenuate the once-around adequately. Too low a choice will result in an inadequate rise time (approximately; Tr = .35/Fxver) and will also require large time constants with attendant large capacitors.A cross-over of 10 Hz will provide approximately 31 dB of attenuation to the fundamental running frequency and give a rise time of 35 ms.

Values (CGS Units)

Torque constant	$Kt = 1$
Back EMF constant	$Kv = 8e^{-3}$
Phase Det. gain	$Kd = 0.35$
Load Inertia	$J_l = 7.5^{e-4}$
Armature resistance	$Ra = 4$
Armature Inductance	$La = 4e^{-3}$
Sense Amp feedback	$Rf = 10k$
Sense resistor	$Rs = 0.2$
Attenuation 1st stage	$K_1 = 0.2$
Sense Amp. gain	$Gi = 5$
Transconductance Gain	$A = 2e^4$
Number Of Pulses/Rev.	$Np = 36$
Transconductance input	$Rspin = 2e^4$
Lead/lag Ratio	$N = 14$

Therefore $\omega_u/\omega_l = 14$;

Making $\omega_x = 62.8$. Using ratios suggested above:

$Kn = KdNpK_1(1 - \beta)\omega_p \times \omega_q \times N/\omega_z$

Figures 12 (a) and 12 (b);

$G_1 = 1.33e^3$; $G_2 = 250$; $G_1G_2 = 3.3325e^5$; $H = 5e^{-4}$; $\beta = 0.66$;

$\omega_a = 1e^3$; $\omega_p = 628$; $\omega_q = 942$; $\omega_z = 6.28$; $\omega_l = 16.$; $\omega_u = 235$

$Kn = 1.185e^6$; Sub. Values in (3):

$$\frac{1185e^6(s + 16.784)(s + 6.28) \times \omega_y}{s^2(s + 942)(s + 628)(s + 235)} \quad (4)$$

Solving at ω_x The Magnitude $= 7.9517e^{-3} \times \omega_y$

Finding Roots of the Current Loop Block

Sub values in equation (2):

$$\frac{6.667e^9}{(s + 3.3343e^6)(s + 7997e^{-4})} \quad (5)$$

The higher frequency pole may be neglected: i.e. divide numerator by both poles and discard the upper.

Solving at ω_x, Magnitude = 31.838

$$\omega_y = \frac{1}{31.838 \times 7.9517e^{-3}} = 3.95$$

Refer To Figure 8.

Choose Cz and Rp.

$Cy = Cz \times \omega_z/\omega_p$; $Rff = RpK_1$; $Cf = 1/(R_{ff}\omega_q)$;

$R_2 = 1/(\omega_y \times C_y)$; $R_l = R_2/(N - 1)$; $Rz = 1/(\omega_z C_z)$;

$C_l = 1/(\omega_u \times R_l)$; Choosing Cz = 0.22 µF and Rp = 300K;

$Rz = 1/(6.28 \times 22e^{-6}) = 720K$;
$Cy = .22e^{-6} \times 6.28/628 = 2.2$ nF;

$R_{ff} = 300e^3 \times 0.2 = 60K$

$R_2 = 1/(3.95 \times 0.22e^{-6}) = 1.15M$;
$R_l = 1.13e^6/13 = 88.5K$;

$C_f = 1/(942 \times 60e^3) = 0.018$ µF;
$C_l = 1/(235 \times 87e^3) = 0.047$ µF

Note K_1: The attenuation factor. Since this stage is followed by an integrator, reducing the first-stage DC gain lowers the value of the integrating time constant, yet does not cause any degradation of performance.

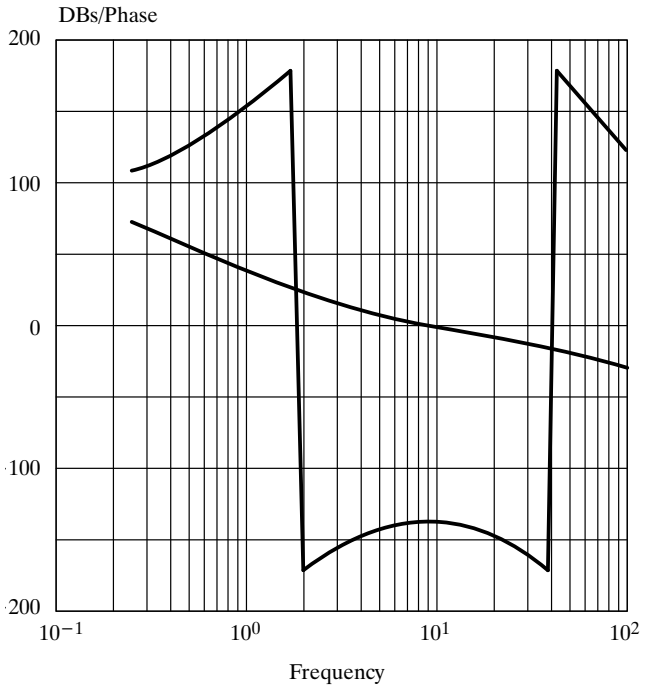


Chart 2. Spindle servo open loop plot.

Snubber Design

Refer to Data Sheet Application Diagram for Si9990CS.

It is necessary to provide a critical or over- damped response in the snubbing structure connected between each phase and the center tap. A ringing response would completely foil the back EMF sensing network, providing an abundance of zero crossings. An over damped response, particularly at too low a frequency, will cause a serious shift of the zero crossing time.

It is therefore the goal to choose a critically damped response for a snubbing system, comprising La, the armature inductance phase to center tap, and damping components C (16 - 18) and R (16 - 18).

The time from the back EMF (switching pulse) to cross-over is represented by 60 electrical degrees of rotor rotation (10 mechanical degrees for a 3-phase 12-pole motor since there are six states per phase cycle).

Calculation of this 30 degree interval:

Time:

$t2 = 60/(RPM \times Npl \times Nph \times 2)$

The choice of resonant frequency must include the time the switching pulse is clamped to either V_{DD} or Ground. Thus t2 is equal to the sum of Toff and one half the period of the resonant frequency of the damping network. The time the switching pulse is clamped to the supply or

ground is a function of the armature current and inductance, Ia and La respectively.

The armature inductor voltage during clamp is

$Ec = V_{DD} - V_b/2$

where Vb is the back EMF voltage at the rotational rate and Vb/2 is one half the voltage representing phase to center tap.

Clamp time:

$Toff = Ia \times La/Ec$

The resonant frequency and the damping resistor can now be calculated.

The maximum half period must be less than: t2 - Toff

Allowing for the exponential decay of a critically damped system, the time to settle to within 2% of final value is

Settle time:

$ts = 4/(0.707 \times \omega n)$

Now n may be calculated, and Cd chosen. Finally, the value for Rd, for critical damping, can be chosen.

Resonating capacitor:

$Cd = 1/(\omega_n^2 \times La)$

The damping resistor $Rd = (4 \times La/Cd)$

Example:

Using values above, assume:

Ia = 0.04 A

Then $t2 = 60/(3600 \times 12 \times 3 \times 2) = 231e^{-6}$;

$Toff = 2e^{-3} \times 0.04/(5 - (8e^{-3} \times RPS \times 2 \times \pi)/2) = 23e^{-6}$

Settling time:

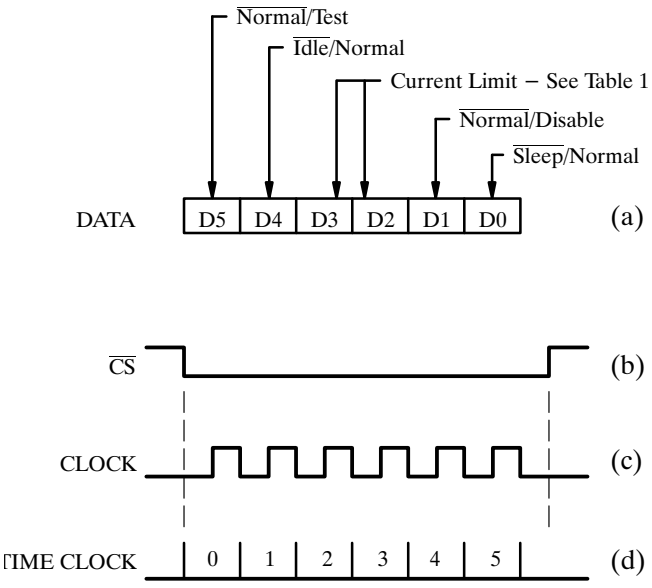
$ts = t2 - Toff = 208e^{-6} = 4/(0.707 \times \omega n)$

$\omega_n = 4/(208e^{-6} \times 0.707) = 2.7e^4$

Then $Cd = 1/(2.7^2 \times 1e^8 \times 2e^{-3}) = 0.68\ \mu F$

$Rd = ((4 \times 2e^{-3})/0.68e^{-6}) = 108\ \Omega s$

NOTE . These value are minimal for ω_n. A higher value for ω_n will yield a smaller Cd but a larger Rd.



(e)

Table 1.

D3	D2	Current
0	0	1 A
0	1	0.6 A
1	0	0.8 A
1	1	0.4 A

Rules
1. D5 is first bit Clock (0)
2. CS goes low when Clock is low
3. CS goes high, latches data in

Figure 13. Serial register timing diagram

Summary

An approach has been presented for the analysis, and subsequent design, of servos for the head actuator arm and spindle motor control, using a Siliconix combination VCM and spindle motor driver IC, the Si9990CS.

Some guidelines, together with explanations, have also been included for design and choice of auxiliary functions, i.e. snubbing, and the components required for acquisition and proper commutation of the spindle motor.

Open loop plots have been included (see chart 1 and chart 2). These indicate a confirmation of performance using the suggested design rules.